

**12V N-CHANNEL ENHANCEMENT MODE MOSFET**
**Product Summary**

$V_{(BR)DSS}$	$R_{DS(ON) \max}$	Package	$I_{D \max}$ $T_A = +25^\circ\text{C}$
12V	10m $\Omega$ @ $V_{GS} = 4.5\text{V}$	U-DFN2020-6 Type E	11A
	12m $\Omega$ @ $V_{GS} = 2.5\text{V}$		10
	14m $\Omega$ @ $V_{GS} = 1.8\text{V}$		9A
	18m $\Omega$ @ $V_{GS} = 1.5\text{V}$		8A
	41m $\Omega$ @ $V_{GS} = 1.2\text{V}$		5A

**Description**

This new generation MOSFET has been designed to minimize the on-state resistance ( $R_{DS(on)}$ ) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

**Applications**

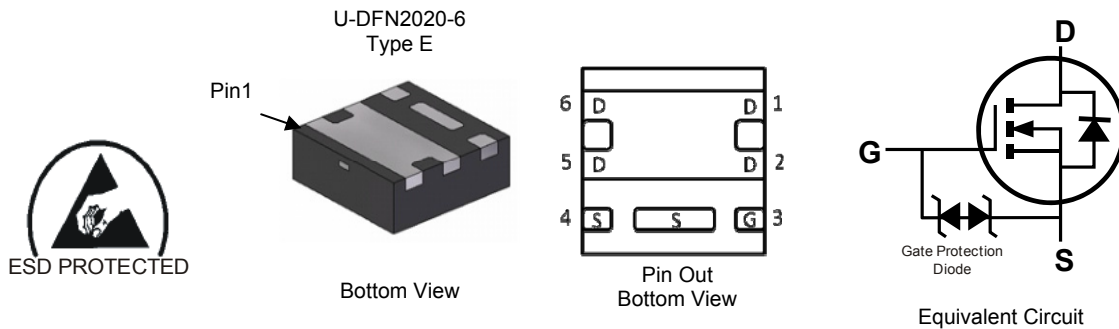
- Load Switching
- Battery Management Application
- Power Management Functions

**Features**

- 0.6mm profile – ideal for low profile applications
- PCB footprint of 4mm<sup>2</sup>
- Low Gate Threshold Voltage
- Fast Switching Speed
- ESD Protected Gate
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

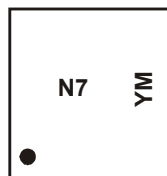
**Mechanical Data**

- Case: U-DFN2020-6 Type E
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – NiPdAu over Copper leadframe. Solderable per MIL-STD-202, Method 208 (64)
- Weight: 0.008 grams (approximate)


**Ordering Information (Note 4)**

Part Number	Marking	Reel size (inches)	Quantity per reel
DMN1019UFDE-7	N7	7	3,000

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
  2. See [http://www.diodes.com/quality/lead\\_free.html](http://www.diodes.com/quality/lead_free.html) for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>

**Marking Information**


N7 = Product Type Marking Code  
 YM = Date Code Marking  
 Y = Year (ex: A = 2013)  
 M = Month (ex: 9 = September)

**Date Code Key**

Year	2011	2012	2013	2014	2015	2016	2017
Code	Y	Z	A	B	C	D	E

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

**Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V <sub>DSS</sub>	12	V
Gate-Source Voltage			V <sub>GSS</sub>	±8	V
Continuous Drain Current (Note 5) V <sub>GS</sub> = 4.5V	Steady State	T <sub>A</sub> = +25°C T <sub>A</sub> = +70°C	I <sub>D</sub>	11 9	A
	t < 5s	T <sub>A</sub> = +25°C T <sub>A</sub> = +70°C	I <sub>D</sub>	14 11	A
Maximum Continuous Body Diode Current			I <sub>S</sub>	3.0	A
Pulsed Drain Current (10µs pulse, duty cycle = 1%)			I <sub>DM</sub>	100	A

**Thermal Characteristics**

Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 5)	T <sub>A</sub> = +25°C	P <sub>D</sub>	0.69	W
	T <sub>A</sub> = +70°C		0.44	
Thermal Resistance, Junction to Ambient (Note 5)	Steady state	R <sub>θJA</sub>	182	°C/W
	t < 5s		118	
Total Power Dissipation (Note 6)	T <sub>A</sub> = +25°C	P <sub>D</sub>	2.17	W
	T <sub>A</sub> = +70°C		1.38	
Thermal Resistance, Junction to Ambient (Note 6)	Steady state	R <sub>θJA</sub>	58	°C/W
	t < 5s		38	
Thermal Resistance, Junction to Case (Note 6)		R <sub>θJC</sub>	10	
Operating and Storage Temperature Range		T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

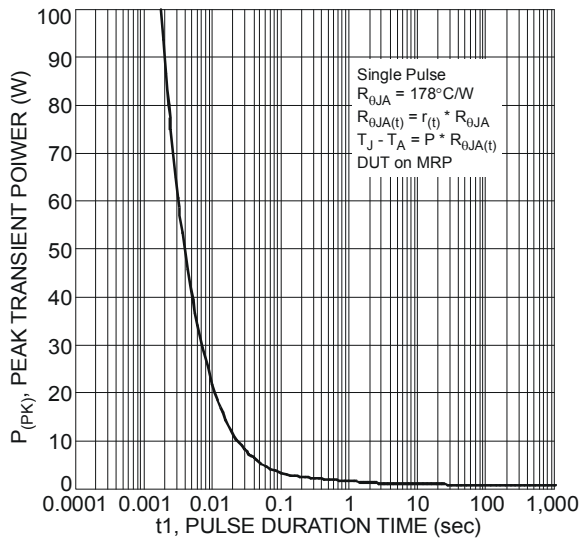


Fig. 1 Single Pulse Maximum Power Dissipation

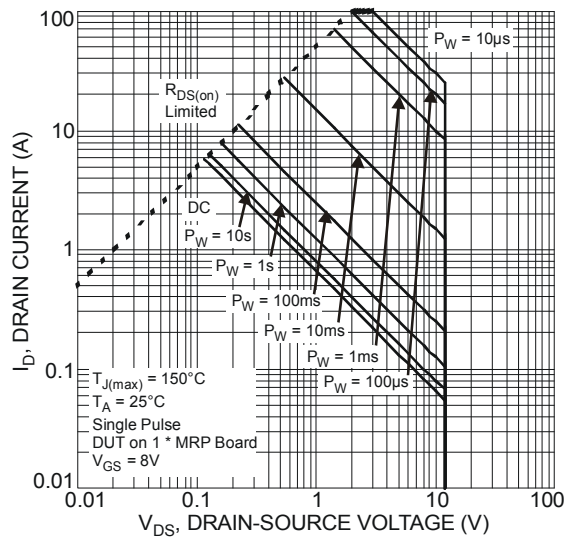


Fig. 2 SOA, Safe Operation Area

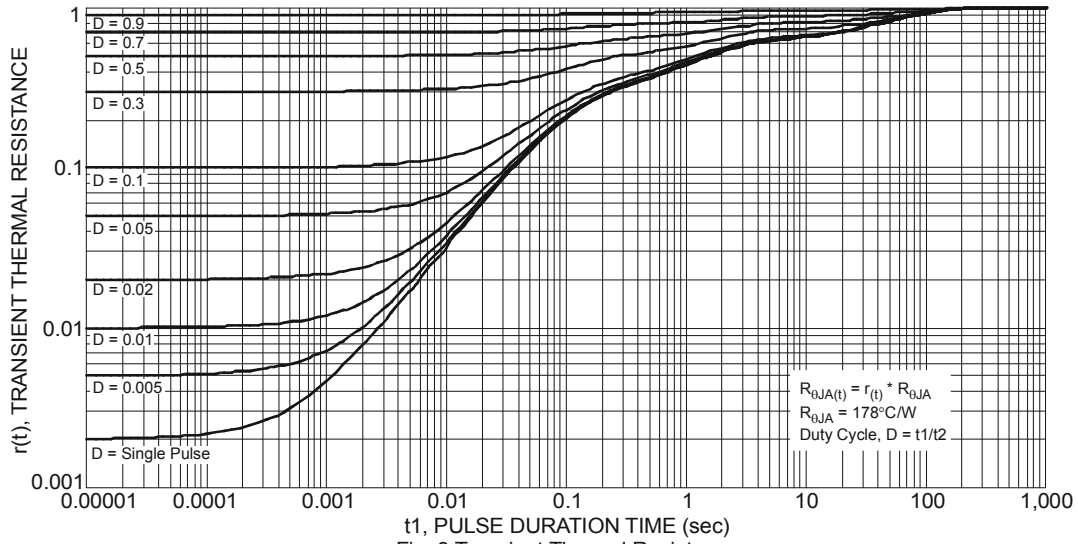


Fig. 3 Transient Thermal Resistance

**Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 7)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	12	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
Zero Gate Voltage Drain Current T <sub>J</sub> = +25°C	I <sub>DSS</sub>	—	—	1	μA	V <sub>DS</sub> = 12V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	—	—	±2	μA	V <sub>GS</sub> = ±8V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 7)</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	0.35	—	0.8	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	—	7	10	mΩ	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 9.7A
			8	12		V <sub>GS</sub> = 2.5V, I <sub>D</sub> = 9A
			10	14		V <sub>GS</sub> = 1.8V, I <sub>D</sub> = 8.1A
			14	18		V <sub>GS</sub> = 1.5V, I <sub>D</sub> = 4.5A
			28	41		V <sub>GS</sub> = 1.2V, I <sub>D</sub> = 2.4A
Forward Transfer Admittance	Y <sub>fs</sub>	—	28	—	S	V <sub>DS</sub> = 4V, I <sub>D</sub> = 9.7A
Diode Forward Voltage	V <sub>SD</sub>	—	0.8	1.2	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 10A
<b>DYNAMIC CHARACTERISTICS (Note 8)</b>						
Input Capacitance	C <sub>iss</sub>	—	2425	—	pF	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0V, f = 1.0MHz
Output Capacitance	C <sub>oss</sub>	—	396	—		
Reverse Transfer Capacitance	C <sub>rss</sub>	—	375	—		
Gate Resistance	R <sub>g</sub>	—	1.1	—	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1MHz
Total Gate Charge (V <sub>GS</sub> = 8V)	Q <sub>g</sub>	—	50.6	—	nC	V <sub>DS</sub> = 4V, I <sub>D</sub> = 10A
Total Gate Charge (V <sub>GS</sub> = 4.5V)	Q <sub>g</sub>	—	27.3	—		
Gate-Source Charge	Q <sub>gs</sub>	—	3.4	—		
Gate-Drain Charge	Q <sub>gd</sub>	—	5.2	—		
Turn-On Delay Time	t <sub>D(on)</sub>	—	7.6	—	ns	V <sub>DD</sub> = 4V, V <sub>GS</sub> = 10V, I <sub>D</sub> = 10A R <sub>G</sub> = 1Ω, R <sub>L</sub> = 0.4Ω
Turn-On Rise Time	t <sub>r</sub>	—	22.2	—		
Turn-Off Delay Time	t <sub>D(off)</sub>	—	57.6	—		
Turn-Off Fall Time	t <sub>f</sub>	—	16.8	—		

- Notes:
- Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
  - Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.
  - Short duration pulse test used to minimize self-heating effect.
  - Guaranteed by design. Not subject to production testing.

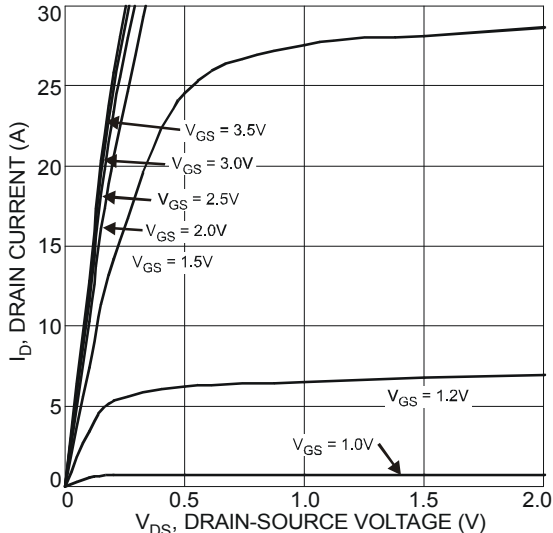


Fig. 4 Typical Output Characteristic

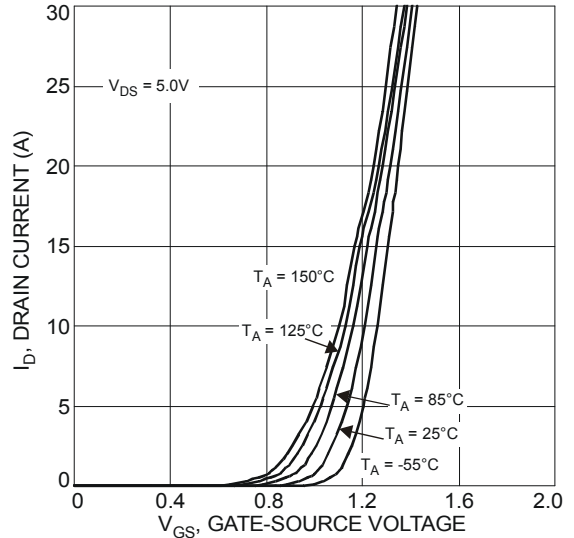


Fig. 5 Typical Transfer Characteristics

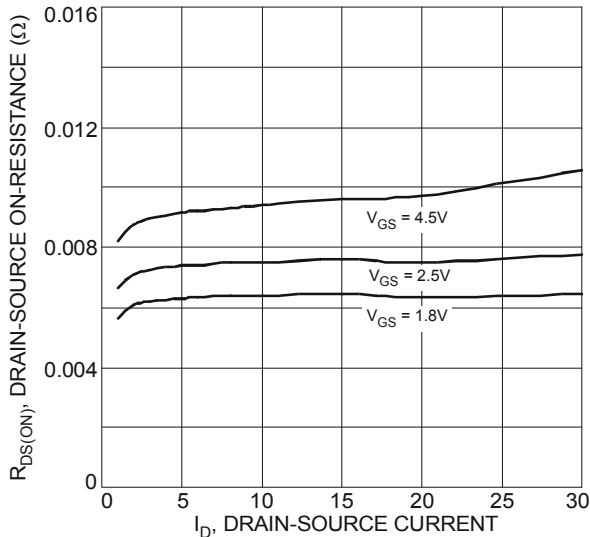


Fig. 6 Typical On-Resistance vs. Drain Current and Gate Voltage

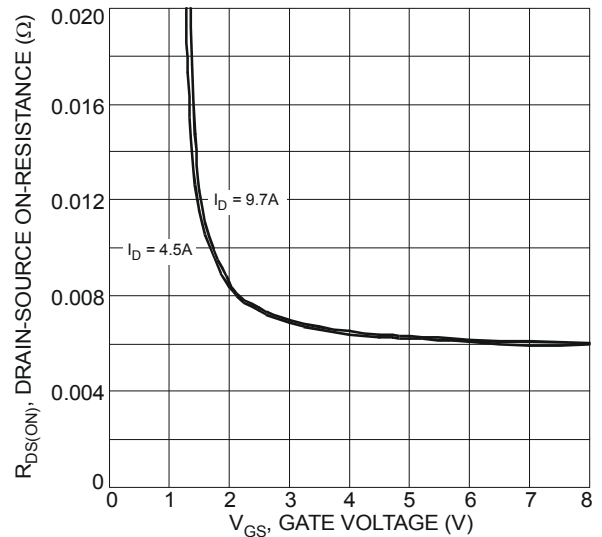


Fig. 7 Typical On-Resistance vs. Gate Voltage

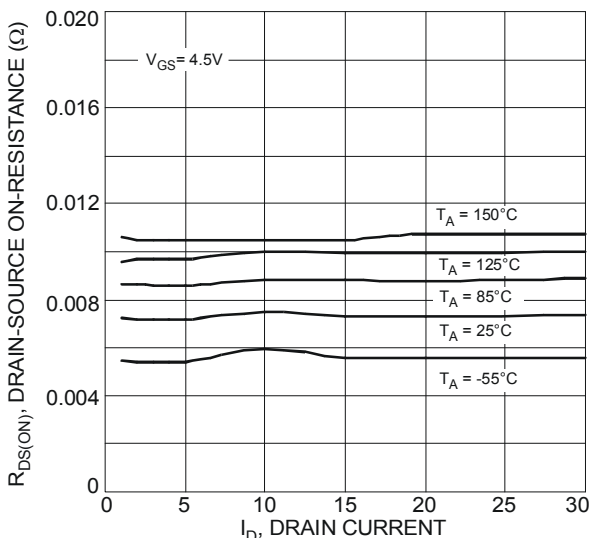


Fig. 8 Typical On-Resistance vs. Drain Current and Temperature

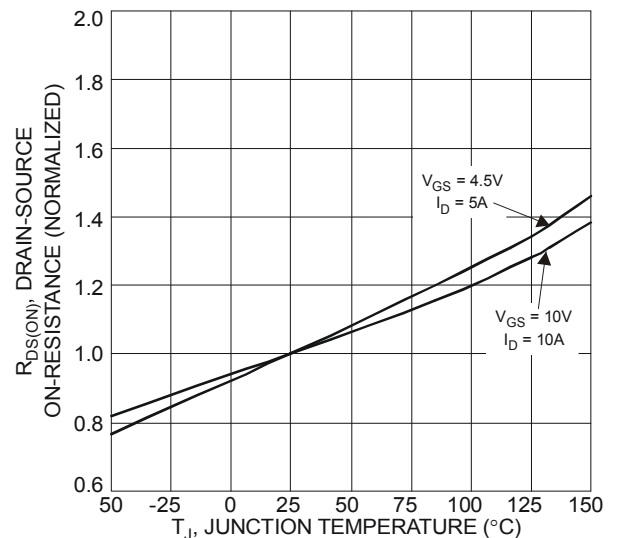


Fig. 9 On-Resistance Variation with Temperature

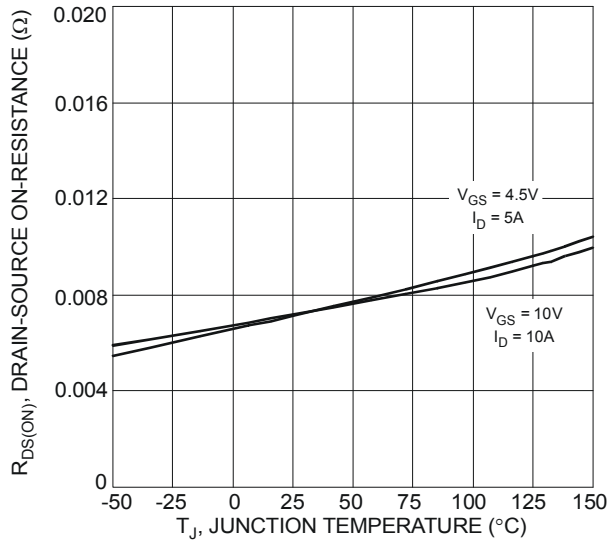


Fig. 10 On-Resistance Variation with Temperature

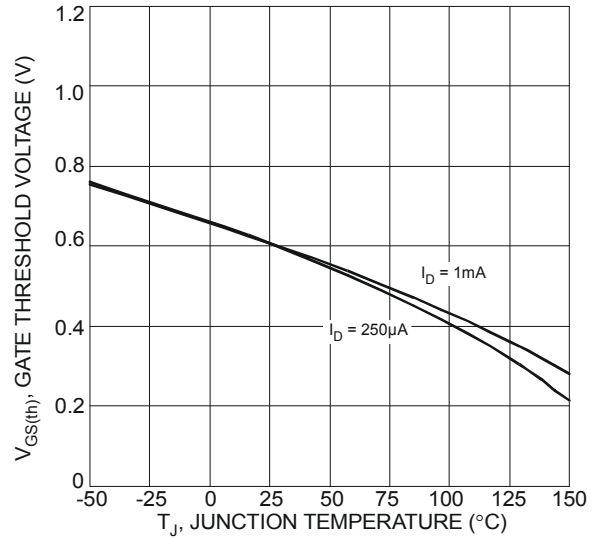


Fig. 11 Gate Threshold Variation vs. Ambient Temperature

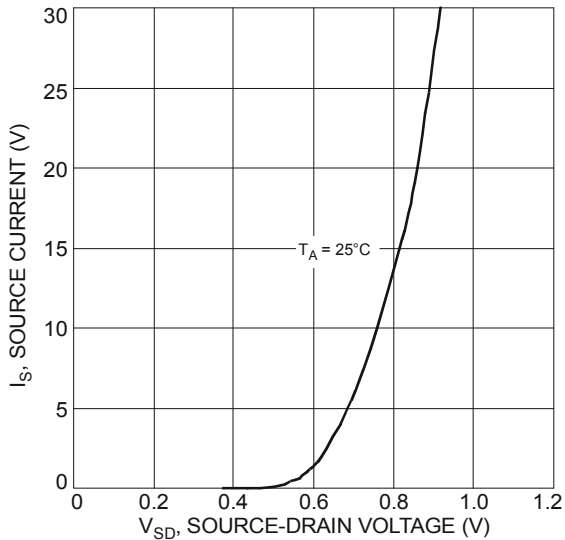


Fig. 12 Diode Forward Voltage vs. Current

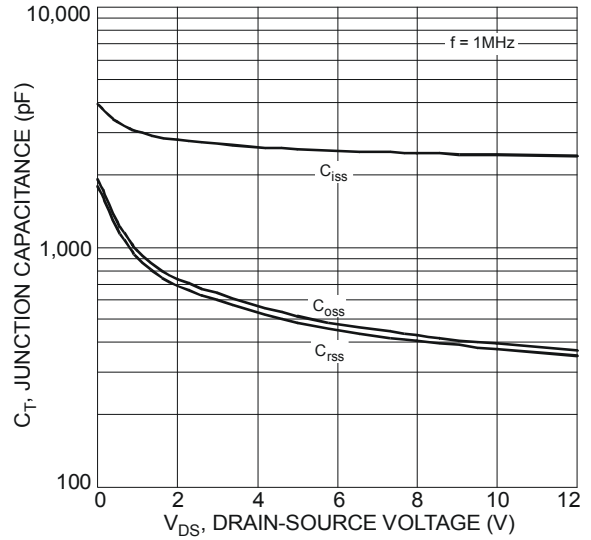


Fig. 13 Typical Junction Capacitance

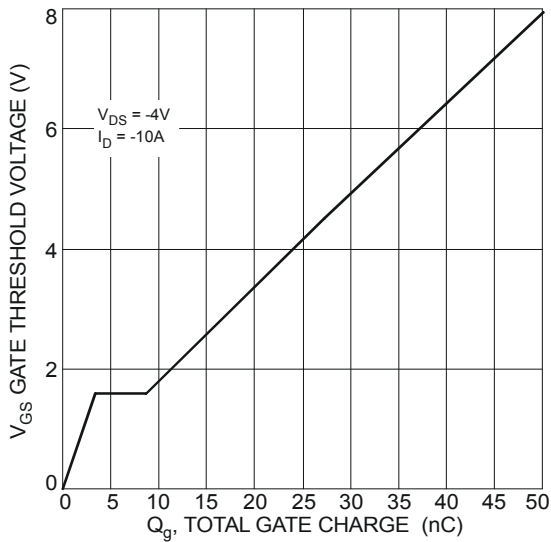
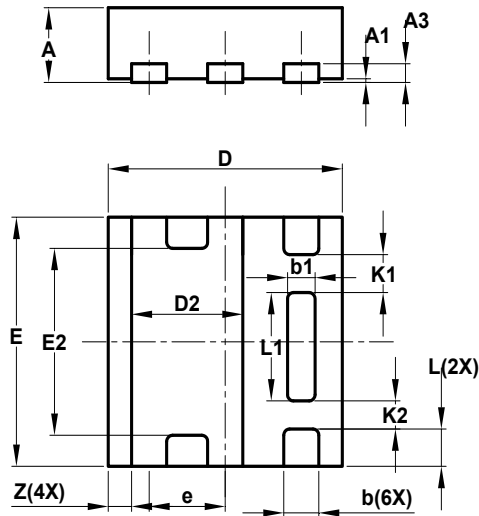


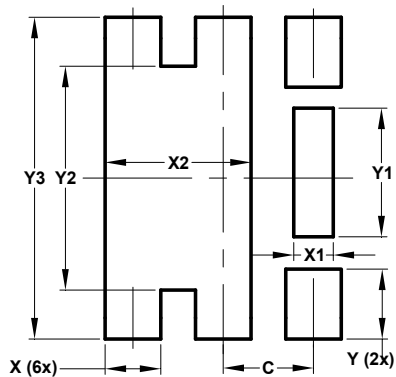
Fig. 14 Gate Charge

**Package Outline Dimensions**



U-DFN2020-6 Type E			
Dim	Min	Max	Typ
A	0.57	0.63	0.60
A1	0	0.05	0.03
A3	—	—	0.15
b	0.25	0.35	0.30
b1	0.185	0.285	0.235
D	1.95	2.05	2.00
D2	0.85	1.05	0.95
E	1.95	2.05	2.00
E2	1.40	1.60	1.50
e	—	—	0.65
L	0.25	0.35	0.30
L1	0.82	0.92	0.87
K1	—	—	0.305
K2	—	—	0.225
Z	—	—	0.20
All Dimensions in mm			

**Suggested Pad Layout**



Dimensions	Value (in mm)
C	0.650
X	0.400
X1	0.285
X2	1.050
Y	0.500
Y1	0.920
Y2	1.600
Y3	2.300

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